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IN THE CLAIMS

1. (Currently amended) A video circuit for processing video signals which show images on a display panel with linear light transition, comprising a gamma correction circuit, a quantizer and a sub-field generator circuit, ~~characterized in that~~wherein a coarse adjustment of the quantization is made in a first random-access memory and a fine adjustment of the quantization is made in a second random-access memory.
2. (Currently amended) A video circuit for processing video signals which display images on a display panel with linear light transition, comprising a gamma correction circuit, a quantizer and a sub-field generation circuit, ~~characterized in that~~wherein most significant bits are quantized in a first random-access memory and least significant bits are quantized in a second random-access memory.
3. (Currently amended) A video circuit for processing video signals which show images on a display panel with linear light transition, comprising a gamma correction ~~circuit~~means, a quantization ~~means~~ and a sub-field generation ~~circuit~~means, ~~characterized in that~~wherein the quantization means is a random-access memory ~~replaces the quantizer.~~
4. (Currently amended) A video circuit as claimed in claim 3, ~~characterized in that~~wherein the random-access memory replaces a dequantizer additionally performs dequantization.

5. (Currently amended) A video circuit as claimed in claim 3, ~~characterized in that~~wherein the random-access memory ~~replaces~~is said gamma correction ~~circuit~~means.

6. (Currently amended) A video circuit as claimed in claim 4, ~~characterized in that~~wherein an inverse gamma circuit is arranged downstream of the ~~dequantizer~~random access memory.

7. (Currently amended) A video circuit as claimed in claim 3, ~~characterized in that~~wherein the random-access memory ~~replaces~~is said a-sub-field generation~~er~~means.

8. (Currently amended) A video circuit as claimed in claim 7, ~~characterized in that~~wherein the-sub-field generation~~er~~applies values are applied to a filter via a conversion ~~meanster~~means and a dequantization ~~meanster~~means.

9. (Currently amended) A video circuit as claimed in claim 8, ~~characterized in that~~wherein the filter applies values to an adder which is situated in an input area of a second signal which represents pixel values of a neighboring line.

10. (Currently amended) A video circuit as claimed in claim 7, ~~characterized in that~~wherein the-sub-field generation~~er~~applies values are applied to the adder via a second conversion ~~meanster~~means and a second dequantization ~~meanster~~means.

11. (Currently amended) A video circuit as claimed in claim 9, ~~characterized in that~~ wherein pixel values of the neighboring line are quantized in a further quantization means in a ~~second random access memory and in the second random access memory~~ and sub-fields are generated in a further sub-field generation means, wherein a further random access memory is said further quantization means and said further sub-field generation means.

12. (Canceled)